



# UNITED STATES PATENT AND TRADEMARK OFFICE

*fw*  
UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,440	11/12/2003	Sharon Duvdevani	U 014858-1	8689
140	7590	03/01/2006	EXAMINER	
LADAS & PARRY 26 WEST 61ST STREET NEW YORK, NY 10023				SETH, MANAV
			ART UNIT	PAPER NUMBER
			2625	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/706,440	DUDEVANI ET AL.
	Examiner	Art Unit
	Manav Seth	2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 27 December 2005.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-15, 18, 20-24 and 27 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-15, 18, 20-24 and 27 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

**DETAILED ACTION**

**Continued Examination Under 37 CFR 1.14**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 27, 2005 has been entered.

**Response to Amendment**

2. Applicant's amendment under 37 C.F.R. 1.116, filed on December 27, 2005 has been considered and entered in full.

3. Applicant's arguments with respect to respective amended claims have been considered but are not moot in view of the new ground(s) of rejection(s) made below, in view of the further consideration of the amended claims.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the

subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8, 12-15 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valesio et al. (FR 2 687 091), further in view of Yamamoto et al., Japanese Patent Publication No. 08-327560, 12/13/1996 and further in view of Aloni et al. (US 5,619,429).

**Regarding claims 1, 5, 12, and 21**, Valesio et al. (“Valesio”) discloses a boundary identifier operative to generate a representation of boundaries of elements in an image which is under inspection (Page 4, para. 7, Page 5; Pages 15-17; Figures 7-8); and a defect identifier operative to receive said representation of boundaries of elements and to analyze at least some locations of at least some boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable locations to identify defects (Pages 4-5; Page 20; Figures 11-13).

Examiner here asserts that a **reference image being an acceptable image** as the image under inspection is compared to it for verification and identification for defect analysis and therefore all the locations on this acceptable image would be acceptable locations. Valesio clearly discloses comparing the series of angles between successive segments with corresponding angles in a theoretical cutout (reference image) to detect defective cutouts, **as agreed by applicant also**, where **these angles are located at different locations on the boundaries**. Valesio further discloses “From the coordinates of the apexes of the polygon which have been identified by the polygonal approximation, one carries out a vectorization phase which consists in calculating the length of each side or segment of the polygon, as well as the angle formed between two successive segments...” (page 16, first paragraph). From above Valesio clearly teaches determining coordinates on the boundary or contour as the first step but Valesio does not specifically teach directly comparing at least coordinates of some locations of at least some boundaries in said representation of boundaries

of elements **itself** with reference to a corresponding region of acceptable location coordinates to identify defects. However, Yamamoto teaches defect detection by comparing at least coordinates of some locations on the boundary or contour of the object under inspection with the coordinates of corresponding locations on the boundary of the reference (criteria) image of the object (Constitution; Detailed Description – page 4 of 5, paragraph [0018]; figures 6, 7 and 9). Therefore, it would have been obvious for one of ordinary skill in the art at the time of invention was made to use Yamamoto's teachings of comparing at least coordinates of some locations on the boundary of the object under inspection to the coordinates of corresponding locations on the boundary of the reference (criteria) image of the object in the invention of Valesio because both references are directed to the same field of endeavor of machine vision for finding defects with respect to boundaries or contours and Yamamoto teaches pinpointing the location of a fault at a higher speed (See Yamamoto, Detailed Description – page 1 of 5, paragraph [0004], last 3 lines; Detailed Description – page 5 of 5, paragraph [0020]) and thus pinpointing the location evidently leads to detection of small defects, which would be difficult using angle comparison.

Valesio and Yamamoto does not appear to recognize the object under inspection being an electrical circuit but also both references do not limit themselves to the specific kind of object under inspection for defect detection (See Valesio, page 1, last 9 lines; See Yamamoto, Detailed Description – page 5 of 5, paragraph [0020], last 3 lines). However, Aloni et al. ("Aloni") discloses inspecting an electrical circuit for defects (Abstract; Col. 2, lines 34-42). Aloni clearly discloses "**comparing at least some of the areas to the corresponding areas of the reference (acceptable) image**" (col. 3, lines 40-48; col. 10, lines 10-18, lines 45-47).

Valesio and Aloni are combinable because they are from the same field of endeavor of machine vision for finding defects. At the time of the invention, it would have been obvious to one

of ordinary skill in the art to have modified the object under inspection to include an electrical circuit. The motivation for doing so would have been because it is well known in the art and it would expand the versatility of the system to encompass inspecting electrical circuits. Also adding more emphasis, Valesio discloses comparing the **locations on** the boundaries to identify the defect, however using Aloni's teachings of comparing **at least some of the areas to the corresponding areas of the reference (acceptable) image** would further add the advantages of comparing at least some areas of at least some boundaries that lie within the boundaries with that of reference image portions to operate to detect certain types of defects, such as pin holes and pin dot type defects, which are somewhat smaller than the selected minimum size. Therefore, it would have been obvious to combine Valesio with Aloni to obtain the invention as specified in claims 1, 12, and 21.

**Regarding claims 2-4, 13-15, and 22-24,** Valesio discloses the boundary identifier operative in hardware and the defect identifier operative in software (Page 4-5, 13, and 16).

**Regarding claim 6,** Valesio discloses the boundaries comprise contours (Figures 7-8, 11-12).

**Regarding claims 7 and 8,** Valesio does not appear to recognize including a putative defect detector. However, Aloni discloses including a putative defect detector operative to identify at least some putative defects (Col. 14, lines 53-65) and to analyze regions associated with the putative defects (Col. 26, lines 40-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to have modified the defect detection disclosed by Valesio to include a putative defect detector. The motivation for doing so would have been because it is a well known

and routinely utilized in the art in order to reduce false alarms. Therefore, it would have been obvious to combine Valesio with Aloni to obtain the invention as specified in claims 7 and 8.

6. Claims 9, 10, 11, 18, 20, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valesio et al. (FR 2 687 091) further in view of Yamamoto et al., Japanese Patent Publication No. 08-327560, 12/13/1996 and further in view of Aloni et al. (US 5,619,429) as applied to claims 1, 8, 12, and 21 above, and further in view of Bachelder (US 5,974,169).

**Regarding claims 9 and 10**, Valesio does not appear to expressly state identifying a region of interest and neither does Yamamoto and Aloni. However, Bachelder discloses identifying bounding boxes or regions (Abstract), thereby a region of interest identifier, and analyzing only those boundaries in the region of interest (Abstract). Valesio, Yamamoto, Aloni, and Bachelder are combinable because they are from the same field of endeavor of machine vision. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have modified the inspection disclosed by Valesio, Yamamoto and Aloni to include a region of interest identifier. The motivation for doing so would have been because it is a well-known methodology used in the art and increases efficiency by limiting the search area. Therefore, it would have been obvious to combine Valesio, Yamamoto and Aloni with Bachelder to obtain the invention as specified in claims 9 and 10.

**Regarding claim 11**, the arguments analogous to those presented above for claims 9 and 10 are applicable to claim 11.

**Regarding claims 18 and 27,** the arguments analogous to those presented above for claim 9 are applicable to claims 18 and 27.

**Regarding claim 20,** the arguments analogous to those presented above for claims 9 and 19 are applicable to claim 20. Bachelder discloses a threshold vicinity comprising an envelope around at least one boundary in the at least one reference image (Figure 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to have modified the threshold vicinity disclosed by Valesio to include an envelope. The motivation for doing so would have been because it accounts for errors arising from any coarse part location error, image acquisition error, or real-world location error (Col. 7, lines 26-32). Therefore, it would have been obvious to combine Valesio, Yamamoto and Aloni with Bachelder to obtain the invention as specified in claim 20.

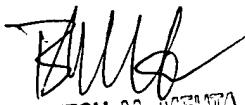
*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manav Seth whose telephone number is (571) 272-7456. The examiner can normally be reached on Monday to Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Manav Seth  
Art Unit 2625  
February 21, 2006



BHAVESH N. MEHTA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600